R05

SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010 LINEAR & DIGITAL IC APPLICATIONS (COMMON TO BME, E.CON.E, ECC, ETM)

Time: 3hours Max.Marks:80

Answer any FIVE questions All questions carry equal marks

- - -

- 1.a) List out the ideal characteristics of an Op-amp.
 - b) With neat block diagram explain the function of various building blocks of an Op-amp?
 - c) Draw the equivalent circuit of an Op-amp.

[3+10+3]

- 2.a) With the help of a neat circuit diagram, explain the operation of a three op-amp instrumentation amplifier and obtain the expression for its output voltage?
 - b) Find R_1 and R_f in the practical integrator (lossy integrator), so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10,000$ rad/sec. Use a capacitance of $0.01\mu F$.
- 3.a) Draw the circuit of a triangular-wave generator, explain its operation and derive expressions for frequency of oscillations?
 - b) Explain the term "VSVS configuration". Design a VCVS low-pass Butterworth second order filter with a cutoff frequency of 5 KHz. Assume necessary data. [8+8]
- 4.a) Explain the operation of Monostable multivibrator using 555 timer and derive expression for its output pulse-width?
 - b) Draw the circuit of Schmitt trigger using 555 timer and explain its operation? [10+6]
- 5.a) With a net sketch explain the operation of an n-bit Weighted Resistor DAC and obtain expression for its output?
 - b) Which is the fastest ADC, explain the operation and discuss its merits & de-merits? [8+8]
- 6.a) Design CMOS transistor circuit for 2-input NOR gate? Explain its operation with the help of Truth-Table?
- b) Draw the schematic circuit of TTL active pull-up NAND gate and explain its operation with the help of Truth-Table? [8+8]
- 7.a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram?
 - b) Design a full subtractor with logic gates? [8+8]
- 8.a) Explain the operation of Synchronous SRAM with the help of its internal Architecture?
- b) Design a conversion circuit to convert a D flip-flop to J-K flip-flop? [8+8]

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R05

SET-2

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010 LINEAR & DIGITAL IC APPLICATIONS (COMMON TO BME, E.CON.E, ECC, ETM)

Time: 3hours Max.Marks:80

Answer any FIVE questions All questions carry equal marks

- - -

- 1.a) Draw the circuit of a triangular-wave generator, explain its operation and derive expressions for frequency of oscillations?
 - b) Explain the term "VSVS configuration". Design a VCVS low-pass Butterworth second order filter with a cutoff frequency of 5 KHz. Assume necessary data. [8+8]
- 2.a) Explain the operation of Monostable multivibrator using 555 timer and derive expression for its output pulse-width?
 - b) Draw the circuit of Schmitt trigger using 555 timer and explain its operation? [10+6]
- 3.a) With a net sketch explain the operation of an n-bit Weighted Resistor DAC and obtain expression for its output?
 - b) Which is the fastest ADC, explain the operation and discuss its merits & de-merits? [8+8]
- 4.a) Design CMOS transistor circuit for 2-input NOR gate? Explain its operation with the help of Truth-Table?
- b) Draw the schematic circuit of TTL active pull-up NAND gate and explain its operation with the help of Truth-Table? [8+8]
- 5.a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram?
- b) Design a full subtractor with logic gates? [8+8]
- 6.a) Explain the operation of Synchronous SRAM with the help of its internal Architecture?
- b) Design a conversion circuit to convert a D flip-flop to J-K flip-flop? [8+8]
- 7.a) List out the ideal characteristics of an Op-amp.
 - b) With neat block diagram explain the function of various building blocks of an Op-amp?
 - c) Draw the equivalent circuit of an Op-amp.

[3+10+3]

- 8.a) With the help of a neat circuit diagram, explain the operation of a three op-amp instrumentation amplifier and obtain the expression for its output voltage?
 - b) Find R_1 and R_f in the practical integrator (lossy integrator), so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10,000$ rad/sec. Use a capacitance of $0.01\mu F$. [8+8]

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R05

SET-3

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010 LINEAR & DIGITAL IC APPLICATIONS (COMMON TO BME, E.CON.E, ECC, ETM)

Time: 3hours Max.Marks:80

Answer any FIVE questions All questions carry equal marks

- - -

- 1.a) With a net sketch explain the operation of an n-bit Weighted Resistor DAC and obtain expression for its output?
 - b) Which is the fastest ADC, explain the operation and discuss its merits & de-merits? [8+8]
- 2.a) Design CMOS transistor circuit for 2-input NOR gate? Explain its operation with the help of Truth-Table?
- b) Draw the schematic circuit of TTL active pull-up NAND gate and explain its operation with the help of Truth-Table? [8+8]
- 3.a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram?
 - b) Design a full subtractor with logic gates?

[8+8]

- 4.a) Explain the operation of Synchronous SRAM with the help of its internal Architecture?
 - b) Design a conversion circuit to convert a D flip-flop to J-K flip-flop?

[8+8]

- 5.a) List out the ideal characteristics of an Op-amp.
 - b) With neat block diagram explain the function of various building blocks of an Op-amp?
 - c) Draw the equivalent circuit of an Op-amp.

[3+10+3]

- 6.a) With the help of a neat circuit diagram, explain the operation of a three op-amp instrumentation amplifier and obtain the expression for its output voltage?
 - b) Find R_1 and R_f in the practical integrator (lossy integrator), so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10,000$ rad/sec. Use a capacitance of $0.01\mu F$. [8+8]
- 7.a) Draw the circuit of a triangular-wave generator, explain its operation and derive expressions for frequency of oscillations?
 - b) Explain the term "VSVS configuration". Design a VCVS low-pass Butterworth second order filter with a cutoff frequency of 5 KHz. Assume necessary data. [8+8]
- 8.a) Explain the operation of Monostable multivibrator using 555 timer and derive expression for its output pulse-width?
 - b) Draw the circuit of Schmitt trigger using 555 timer and explain its operation? [10+6]

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R05

SET-4

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010 LINEAR & DIGITAL IC APPLICATIONS (COMMON TO BME, E.CON.E, ECC, ETM)

Time: 3hours Max.Marks:80

Answer any FIVE questions All questions carry equal marks

- - -

- 1.a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram?
 - b) Design a full subtractor with logic gates?

[8+8]

- 2.a) Explain the operation of Synchronous SRAM with the help of its internal Architecture?
 - b) Design a conversion circuit to convert a D flip-flop to J-K flip-flop?

[8+3]

- 3.a) List out the ideal characteristics of an Op-amp.
 - b) With neat block diagram explain the function of various building blocks of an Op-amp?
 - c) Draw the equivalent circuit of an Op-amp.

[3+10+3]

- 4.a) With the help of a neat circuit diagram, explain the operation of a three op-amp instrumentation amplifier and obtain the expression for its output voltage?
 - b) Find R_1 and R_f in the practical integrator (lossy integrator), so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10,000$ rad/sec. Use a capacitance of $0.01\mu F$.
- 5.a) Draw the circuit of a triangular-wave generator, explain its operation and derive expressions for frequency of oscillations?
 - b) Explain the term "VSVS configuration". Design a VCVS low-pass Butterworth second order filter with a cutoff frequency of 5 KHz. Assume necessary data. [8+8]
- 6.a) Explain the operation of Monostable multivibrator using 555 timer and derive expression for its output pulse-width?
 - b) Draw the circuit of Schmitt trigger using 555 timer and explain its operation? [10+6]
- 7.a) With a net sketch explain the operation of an n-bit Weighted Resistor DAC and obtain expression for its output?
 - b) Which is the fastest ADC, explain the operation and discuss its merits & de-merits? [8+8]
- 8.a) Design CMOS transistor circuit for 2-input NOR gate? Explain its operation with the help of Truth-Table?
- b) Draw the schematic circuit of TTL active pull-up NAND gate and explain its operation with the help of Truth-Table? [8+8]

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